CLAIMS

1-6. (Cancelled)

7. (Currently amended) A processor comprising:

a processor core; and

a ~~first~~ cache memory for general-purpose operation of the processor core; ~~and~~ ~~a second cache memory dedicated to a first computer process~~ wherein the processor is to evaluate the cache memory when a first computer process associated with a thread results in a cache operation for the cache memory to determine whether a dedicated cache for the thread exists in the cache memory and, if a dedicated cache does not exist, whether a dedicated cache for the thread is needed; and

wherein if the processor determines that a dedicated cache for the thread does not exist and a dedicated cache is needed for the thread, the processor is to create a dedicated sector in the cache memory, the resulting cache memory having a first sector for the general purpose operation and a second sector dedicated to the thread.

8. (Original) The processor of claim 7, wherein first computer process is a multi-media process.

9. (Currently amended) The processor of claim 7, wherein the first computer process is allocated ~~certain~~ a subset of the computing cycles of the processor.

10. (Cancelled)

11. (Currently amended) The processor of claim [[10]] 7, wherein ~~the second cache memory may be dynamically created or eliminated~~ if the dedicated cache exists for the thread of the computer operation, the processor makes a determination whether the dedicated cache should be eliminated.

12. (Currently amended) The processor of claim [[10]] 7, wherein ~~the size of second cache memory sector may~~ if the p be dynamically modified.

13. (Currently amended) A system comprising:

a bus;

a processor coupled to the bus; and

a ~~first~~ cache memory to support ~~general-purpose operation~~ operations for the processor; ~~and~~

~~a second cache memory dedicated to a first program thread~~.

wherein the processor is to evaluate the cache memory when a first computer process associated with a first program thread results in a cache operation for the cache memory to determine whether a dedicated cache for the first program thread exists in the cache memory and, if a dedicated cache does not exist, whether a dedicated cache for the first program thread is needed; and

wherein if the processor determines that a dedicated cache for the first program thread does not exist and a dedicated cache is needed for the first program thread, the processor is to create a dedicated sector in the cache memory, the resulting cache memory having a first cache sector for the general

purpose operation and a second cache sector dedicated to the first program thread.

14. (Original) The system of claim 13, wherein first program thread is a multi-media process.

15. (Currently amended) The system of claim 13, wherein the first program thread is allocated ~~certain~~ a subset of the computing cycles of the processor.

16. (Cancelled)

17. (Currently amended) The system of claim 16, wherein the processor is to dynamically eliminate the second cache memory ~~may be dynamically created or eliminated~~ sector.

18. (Currently amended) The system of claim 16, wherein the processor is to dynamically change the size of the second cache ~~memory sector may be dynamically modified~~ sector.

19. (Currently amended) The system of claim 13, wherein the first cache ~~memory~~ sector and the second cache ~~memory~~ sector are included in the processor.

20. (Currently amended) A method comprising:

performing a computer operation associated with a first thread, the computer operation resulting in an operation for a cache memory;

determining whether a dedicated cache exists for the first thread;

upon a determination that a dedicated thread exists for the first thread, performing the cache operation in the dedicated cache; and

upon a determination that a dedicated cache does not exist for the first thread, determining whether a dedicated cache is needed for the first thread.

~~storing data relating to a plurality of computer operations in a first cache memory; and~~

~~storing data regarding a first computer process in a dedicated second cache memory.~~

21. (Currently amended) The method of claim 20, further comprising creating the ~~second cache~~ dedicated cache memory in the cache memory.

22. (Currently amended) The method of claim 20, further comprising determining that the dedicated cache memory is an incorrect size and changing the size of the ~~second~~ dedicated cache memory.

23. (Currently amended) The method of claim 20, further comprising determining that the dedicated cache memory is not needed and eliminating the ~~second~~ dedicated cache memory.

24. (Currently amended) The method of claim 20, further comprising flushing the ~~first~~ cache memory without flushing the ~~second~~ dedicated cache memory.

25. (Currently amended) A machine-readable medium having stored thereon data representing sequences of instructions that, when executed by a processor, cause the processor to perform operations comprising:

performing a computer operation associated with a first thread, the computer operation resulting in an operation for a cache memory;

determining whether a dedicated cache exists for the first thread;

upon a determination that a dedicated thread exists for the first thread, performing the cache operation in the dedicated cache; and

upon a determination that a dedicated cache does not exist for the first thread, determining whether a dedicated cache is needed for the first thread.

~~storing data relating to a plurality of computer operations in a first cache memory; and~~

~~storing data regarding a first computer process in a dedicated second cache memory.~~

26. (Currently amended) The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations comprising creating the ~~second~~ dedicated cache in the cache memory.

27. (Currently amended) The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations comprising determining that the dedicated cache is an incorrect size and changing the size of the ~~second cache memory~~ dedicated cache.

28. (Currently amended) The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations comprising determining that the dedicated cache memory is not needed and eliminating the ~~second cache memory~~ dedicated cache.

29. (Currently amended) The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations comprising flushing the ~~first~~ cache memory without flushing the ~~second cache memory~~ dedicated cache.